Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CLOCK B**
2. **Q4B**
3. **Q3A**
4. **Q2A**
5. **Q1A**
6. **RESET A**
7. **DATA A**
8. **VSS**
9. **CLOCK A**
10. **Q4A**
11. **Q3B**
12. **Q2B**
13. **Q1B**
14. **RESET B**
15. **DATA B**
16. **VDD**

**.087”**

**.070”**

**2 1 16**

**15**

**14**

**13**

**12**

**11**

**3**

**4**

**5**

**6**

**7**

**8 9 10**

**CD4015B**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4015B**

**APPROVED BY: DK DIE SIZE .070” X .087” DATE: 3/9/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: CD4015BH**

**DG 10.1.2**

#### Rev B, 7/19/02